Letters

Design and Implementation of a Sensorless Multilevel Inverter With Reduced Part Count

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***Abstract*—This letter proposes a single-phase nine-level (9L) inverter topology suitable for grid-connected renewable energy systems. The proposed inverter is realized using a T-type neutral-point-clamped inverter connected in cascade to a floating capacitor (FC) H-bridge. Additionally, two low-frequency switches are added across the dc-link enabling the inverter to generate a 9L waveform. A sensorless voltage control based on redundant switching state is developed and embedded with PWM controller, which is responsible for regulating the FC voltage at one-quarter of the dc source voltage. The proposed PWM technique employs the generation of 9L waveform without using any voltage sensor, thereby reducing the complexity of the overall control scheme. This, in turn, will make the overall system appealing for various industrial applications. In comparison to conventional and recent topologies, generation of the 9L waveform using a lower number of components is the notable contribution. Another important feature of the proposed inverter is that if FC H-bridge fails, it can be bypassed, and the inverter can still operate as a 5L inverter at its nominal power rating. Furthermore, a comprehensive comparison study is included which confirms the merits of the proposed inverter against those of other state-of-the-art topologies. Finally, simulation and experimental results are included for validating the feasibility of the proposed system.**

***Index Terms*—Floating capacitor (FC), nine-level (9L) inverter, power quality, sensorless voltage control.**

I. Introduction

THE depletion of fossil fuels, rising environmental concerns and day-by-day increasing demand for electrical energy has elevated the need for generating energy from alternate sources. Wind and solar photovoltaic (PV) technology has gained a lot of attention among renewable energy sources as they are environment-friendly. This quick growth has created an arena in view of exploiting the wind and PV energy fully, wherein many expeditious technologies in the field of power electronic converter structures for enabling the integration of renewable energy based system for electric power generation have emerged [1], [2].

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In general, for low power and residential applications with a rating less than 10 kW, a single-phase grid-connected inverter is preferred [3], [4]. A three-level (3L) inverter proposed by Nabae *et al.* [5] is one of the standard topologies that has gained attention. However, factors like increased switching frequency, acoustic noise and power loss necessitated the use of multilevel dc–ac power converters with voltage levels greater than three [6]. The significant features of multilevel inverters, like their ability to handle high voltages with reduced stress across individual devices, low switching and conduction losses, transformerless operation and enhanced power quality with lower harmonic distortion have made them an attractive and competent solution for many applications [7], [8]. Currently, some of the popular topologies that are considered as applicable multilevel inverters are the cascaded H-bridge (CHB), neutral-point-clamped (NPC), modular multilevel converter (MMC), a flying capacitor, and their variants [9], [10]. Increasing the number of levels intending to reduce harmonic distortion with superior waveform quality profoundly impacts the inverter size and cost. In this context, several innovative inverter topologies with a claim of a reduced part count (RPC) are reported in literature [11], [12].

The topology proposed in [13] can generate a 7L output voltage with RPC. However unbalancing in the front-end capacitor voltage divider circuit increases the control complexity which is not addressed. A detailed survey of applicable 9L inverters for distributed generation is presented in [14]. Also, a new topology with a cascade connection of 5L active neutral-point-clamped (ANPC) and 3L floating capacitor (FC) H-bridge is proposed. A combination of CHB with FC H-bridge presented in [15] consists of one dc source and eight switches only. However, regulation of FC voltage at $1/3V_{\rm dc}$ requires additional circuit, while mere experimental results are presented. A configuration which includes 5L double flying capacitor multicell (DFCM) converters cascaded with FC H-bridge is recommended in [16] to overcome the increased diversity factor in a DFCM converter. A 9L cross-connected intermediate level unit integrated with ANPC is introduced in [17]. Most of these topologies are hybrid combinations of one or more converter families (NPC, FC, and CHB). Many such hybridizations resulting in 9L RPC inverter are reported in literature [18]–[20]. Although for identical voltage levels, the topologies mentioned require a lesser number of components, the drawbacks associated are high-frequency switching of power devices, a lot of feedback

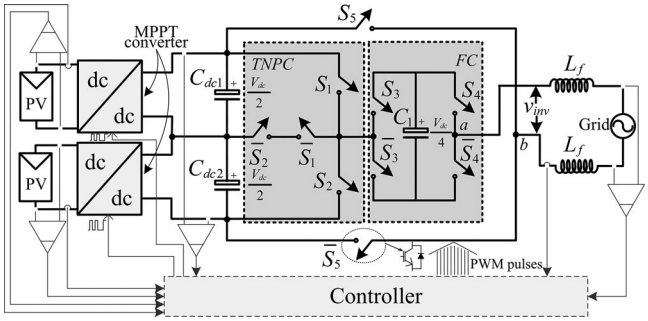

Fig. 1. Circuit topology of the proposed inverter.

sensors, increased voltage diversity factor and higher control complexity.

From the industrial point of view, use of a high number of part counts in conventional multilevel inverters increases both the intricacy of the circuitry as well as the complexity of the control scheme involved. This eventually leads to higher cost implications and reduced reliability. Therefore, this letter presents a novel hybrid 9L inverter on the basis of reduced part count and using sensorless PWM technique. A detailed comparison is carried out and is presented to illustrate the distinctive characteristics and benefits of the proposed inverter. First, a single-phase grid-connected system comprising the proposed topology is simulated, and then its loss evaluation is manifested through the simulation results. Further, a laboratory scale prototype of the proposed inverter is built. Simulation waveforms and experimental measurements are elucidated both for steady-state and transient operating conditions to validate the proposed hybrid inverter.

II. Proposed 9L Inverter Operating Principle and Control

A. Circuit Description

Fig. 1 shows the power circuit topology of the proposed 9L inverter. It comprises mainly three units; a 3L TNPC cascaded with 3L FC H-bridge unit and two low-frequency switches (LFS) across the dc-link. With $V_{\rm dc}$ being the total input voltage, the voltages across the dc-link capacitors and FC are equal to $V_{\rm dc}/2$ and $V_{\rm dc}/4$, respectively. The idea of cascading TNPC with FC yields in the following advantage of fewer number of power devices, power diodes, and capacitors, and more importantly it is modular in comparison with other inverters generating same number of levels. The resulting topology is adaptable for a higher number of voltage levels by appending more FC H-bridges as per the level requirement. Ideally, the inverter is capable of generating nine levels of output voltage: $\pm V_{\rm dc}$, $\pm 3V_{\rm dc}/4$, $\pm V_{\rm dc}/2$, $\pm V_{\rm dc}/4$, 0. At a first glance, the cascade configuration of TNPC and FC with two LFS might seem inconspicuous. In the absence of a LFS unit, with the dc-link midpoint being the return path for the output current, the cascade combination of TNPC and FC can only generate five levels: $\pm V_{\rm dc}/2$, $\pm V_{\rm dc}/4$, 0. Also, in this case, the peak values of the output voltages are only half of the dc-link voltage, i.e., $\pm V_{\rm dc}/2$. However, with inclusion of two LFS units across the dc-link, it is possible to obtain full value of the dc-link voltage, i.e., $\pm V_{\rm dc}$ for both positive and negative half cycles of the output voltage. As a result, it can synthesize output voltage with additional levels: $\pm V_{\rm dc}$ and $\pm 3V_{\rm dc}/4$. For this, power switches are to be gated appropriately in a sequence. Table I summarizes all the possible switching combinations and their effect on the FC voltage. Assuming the devices to be ideal, FC is large enough and load as pure resistive, the active current path over a positive half cycle of the output voltage for each level is obtained as follows:

1) Maximum positive output ($V_{\rm dc}$): This voltage is designated as L_{4^+}. Switches S_1, S_3, and S_4 are ON, connecting the terminal a to $V_{\rm dc}$, and $\bar{S}_5$ is ON, connecting the terminal b to ground. Thus, the voltage across the load is $V_0 = V_{\rm dc} + 0 = V_{\rm dc}$.
2) Three-fourth positive output ($3V_{\rm dc}/4$): Two switching combinations are available. For L_{31^+}, switches $\bar{S}_1$, $\bar{S}_2$, $\bar{S}_3$, and S_4 are ON, connecting the terminal a to $V_{\rm dc}/4$, and $\bar{S}_5$ is ON, connecting the terminal b to ground. Thus the voltage across the load is $V_0 = V_{\rm dc}/2 + V_{\rm dc}/4 = 3V_{\rm dc}/4$. For L_{32^+}, switches S_1, $\bar{S}_2$, S_3, and $\bar{S}_4$ are ON, connecting the terminal a to $-V_{\rm dc}/4$, and $\bar{S}_5$ is ON, connecting the terminal b to ground. Thus the voltage across the load is $V_0 = V_{\rm dc} - V_{\rm dc}/4 = 3V_{\rm dc}/4$.
3) Half-level positive output ($V_{\rm dc}/2$): This voltage is designated as L_{2^+}. Switches $\bar{S}_1$, $\bar{S}_2$, S_3, and S_4 are ON, connecting the terminal a to $V_{\rm dc}/2$, and $\bar{S}_5$ is ON, connecting the terminal b to ground. Thus the voltage across the load is $V_0 = V_{\rm dc}/2 + 0 = V_{\rm dc}/2$.
4) One-fourth positive output ($V_{\rm dc}/4$): Two switching combinations are available. For L_{11^+}, switches S_2, $\bar{S}_3$, and S_4 are ON, connecting the terminal a to $V_{\rm dc}/4$, and $\bar{S}_5$ is ON, connecting the terminal b to ground. Thus, the voltage across the load is $V_0 = 0 + V_{\rm dc}/4 = V_{\rm dc}/4$. For L_{12^+}, switches S_1, $\bar{S}_2$, S_3, and $\bar{S}_4$ are ON, connecting the terminal a to $+V_{\rm dc}/4$, and $\bar{S}_5$ is ON, connecting the terminal b to ground. Thus, the voltage across the load is $V_0 = V_{\rm dc}/2 - V_{\rm dc}/4 = V_{\rm dc}/4$.

TABLE I
Switching States and Their Impact on FC Voltage of the Proposed Inverter

States	S_1	S_2	S_3	S_4	S_5	Output voltage	FC voltage
L_{4+}	1	0	1	1	0	$V_{\rm dc}$	No effect
L_{31+}	0	0	0	1	0	$3V_{\rm dc}/4$	Discharging
L_{32+}	1	0	1	0	0	$3V_{\rm dc}/4$	Charging
L_{2+}	0	0	1	1	0	$V_{\rm dc}/2$	No effect
L_{11+}	0	1	0	1	0	$V_{\rm dc}/4$	Disharging
L_{12+}	0	0	1	0	0	$V_{\rm dc}/4$	Charging
L_{0+}	0	1	1	1	0	0	No effect
L_{0-}	1	0	1	1	1	0	No effect
L_{11-}	1	0	1	0	1	$-V_{\rm dc}/4$	Discharging
L_{12-}	0	0	0	1	1	$-V_{\rm dc}/4$	Charging
L_{2-}	0	0	1	1	1	$-V_{\rm dc}/2$	No effect
L_{31-}	0	0	1	0	1	$-3V_{\rm dc}/4$	Discharging
L_{32-}	0	1	0	1	1	$-3V_{\rm dc}/4$	Charging
L_{4-}	0	1	1	1	1	$-V_{\rm dc}$	No effect

5) Zero output: Two switching combinations are available. For L_{0^+}, switches S_2, S_3, and S_4 are ON, connecting the terminal a to ground, and $\bar{S}_5$ is ON, connecting the terminal b to ground. For L_{0^-}, switches S_1, S_3 and S_4 are ON, connecting the terminal a to $V_{\rm dc}$, and S_5 is ON, connecting the terminal b to $V_{\rm dc}$. In both cases, the terminal ab is short circuited, and the voltage across the load is zero.

The number of power switches conducting the circuit current plays a crucial role in determining the efficiency of the inverter. In the proposed inverter, this figure ranges from four switches to five switches, with one of the switches operating at low-frequency (50 Hz). Consequently, the number of active power switches in the circuit current path is lower in comparison to [21], [22], and hence, this topology has a better efficiency.

B. Sensorless Voltage Balancing of FC

One of the key targets of the proposed inverter control is to regulate FC voltage to one-quarter of the dc source voltage. It is clear from Table I that 14 switching states can provide different paths for load current among which ten states are beneficial in producing five levels, comprising $-3V_{\rm dc}/4$, $-V_{\rm dc}/4$, 0, $V_{\rm dc}/4$, and $3V_{\rm dc}/4$. This implies that there are a few switching states that provide a different path for the current through the system while maintaining the same output voltage level. This redundancy in switching states can be effectively utilized for charging and discharging the FC voltage, thereby allowing it to balance around its requisite value. In order to arrive at an efficient design for the PWM controller, the effect of each possible and valid switching state on FC voltage is studied and reported in Table I. It is worth mentioning here that all the switching states do not result in deviation of the FC voltage. At each level of output voltage (except $\pm V_{\rm dc}/2$ and $\pm V_{\rm dc}$), switching state redundancies exist. Contrary to the general philosophy of voltage balancing using voltage sensor for sensing the FC voltage, a sensorless approach as proposed by [23] is slightly adapted and used in this proposed topology. This makes the proposed system more cost effective. In order to stabilize and regulate the FC voltage, it is decided to charge FC during the positive half cycles of the fundamental voltage (viz., switching states L_{12^+} and L_{32^+}) and discharge during the negative half cycles (viz., switching states L_{11^-} and L_{31^-}), respectively. The charging and discharging time period of the FC is kept similar to one complete cycle of the fundamental output voltage, which leads to equalization of energy into and from the FC in every cycle of the output voltage and consequently, the voltage across the FC is maintained at the desired level in all conditions. Regarding the sizing of FC, the parameters to be considered for its design are; voltage ripple ($\Delta V_{\rm C}$), switching frequency ($f_{\rm sw}$), and the maximum value of load current ($I_{\rm pk}$). Thus, its value is calculated using the following formula:

$$C = \frac{I_{\rm pk}}{\Delta V_{\rm C} \times f_{\rm sw}}. \tag{1}$$

Selection of a higher switching frequency leads to shorter charging/discharging time thereby enhancing the balancing performance. While the voltage balancing concept is dependent on symmetric charging/discharging times, other factors like grid voltage distortion in the case of grid-connected renewable systems and the nonidealities present in the real power devices/components do not affect its performance significantly.

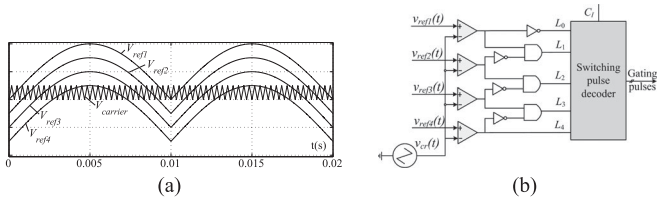

Fig. 2. (a) Multilevel PWM reference and carrier signals. (b) PWM modulator.

TABLE II
BINARY INTERPRETATION OF THE LOGIC EMBEDDED IN SWITCHING PULSE DECODER

					Switching state to be selected	
L_0	L_1	L_2	L_3	L_4	$C_I = 1$	$C_I = 0$
1	0	0	0	0	L_{0^+}	L_{0^-}
0	1	0	0	0	L_{12^+}	L_{11^-}
0	0	1	0	0	L_{2^+}	L_{2^-}
0	0	0	1	0	L_{32^+}	L_{31^-}
0	0	0	0	1	L_{4^+}	L_{4^-}

C. Multilevel PWM With Integrated Voltage Balancing Control

To reduce the implementation issues related to FC voltage balancing and to generate a multilevel output voltage, a novel PWM modulation technique developed from [24], [25] is introduced. In contrast to [23], the proposed PWM technique employs a sensorless FC voltage balancing control in which four reference signals ($V_{\rm ref1}(t)$, $V_{\rm ref2}(t)$, $V_{\rm ref3}(t)$, and $V_{\rm ref4}(t)$) are compared with a single carrier signal ($V_{\rm carrier}(t)$). These reference signals differ only in terms of an offset added, apart from that they all are in phase, and have the same frequency and amplitude. The value of the offset added is equal to the maximum amplitude of the $V_{\rm carrier}(t)$. Since the proposed inverter utilizes four reference signals, the modulation index is given by

$$m_a = \frac{V_m}{4 \times V_c} \tag{2}$$

where V_m is the peak-to-peak value of the reference signal and V_c is the peak-to-peak value of the carrier signal.

Fig. 2(a) shows the sinusoidal reference signals and the carrier signal while Fig. 2(b) depicts the schematic diagram of the developed PWM modulator. Each of the four reference signals is compared with the carrier for generating the PWM signals. By employing suitable logic operation on the output of the comparators, the level of output voltage to be generated is extracted. The binary interpretations of the logic associated with voltage levels are shown in Table II. C_I is the cycle identifier; $C_I = 1/0$, indicates that the levels to be generated correspond to positive/negative half cycle of the fundamental output voltage respectively. The level information data ($L_0, L_1, L_2, L_3,$

TABLE III
COMPARISON OF THE PROPOSED INVERTER WITH OTHER TOPOLOGIES

	Multilevel inverter type										
	[5]	[14]	[16]	[17]	[19]	[20]	[21]	[26]	[27]	[28]	Proposed
LSR	0.56	0.75	0.9	0.64	0.64	0.75	0.56	0.9	0.75	0.64	0.9
Number of FCs	–	2	2	2	2	3	–	2	3	3	1
Number of DC sources	8	2	1	2	2	2	4	2	2	2	1
Voltage diversity factor	–	0.75	0.75	0.75	0.75	0.375	–	0.58	3	0.625	0.25
Total blocking voltage (p.u.)	6	7	3.5	7.5	9	3.5	6	8	6	4	2.5
% Reduction of devices	37.5	16.66	0	28.57	28.57	16.66	37.5	0	16.66	28.57	–
Number of sensors	–	3	0	3	3	4	–	3	4	4	0

and L_4) forms the row index and the cycle identifier output forms the column index of the lookup table. This data is stored in the switching pulse decoder to select a particular switching state. For example, $L_3 = 1$ and $C_I = 1$ indicates that output voltage level to be generated is $3V_{\rm dc}/4$ and output voltage is in its positive half cycle. Hence, the switching state L_{32^+} is selected and gating pulses are generated accordingly. Moreover, redundant switching states L_{0^+} and L_{0^-} are used for generating level zero of output voltage during its positive and negative half cycles respectively, to minimize switching losses (owing to switching transitions). As mentioned earlier, application of this PWM technique generates a 9L output voltage waveform at the output without need for any voltage sensor, thereby reducing complex control computations. Practical implementation of this method is simple and economical since the PWM is realized using a single high-frequency carrier signal, level-shifted sinusoidal reference signals, logic gates, and a lookup table. Furthermore, this technique is independent of modulation index, system nonlinearities, switching frequency, and feedback measurement sensors.

D. Comparative Study

A generalized comparison, taking into consideration various prominent figures of merit of the proposed inverter, with some of the recent classic multilevel topologies, is drawn and tabulated in Table III. The proposed inverter has the highest level/switch ratio (LSR) except the topologies presented in [16] and [26] wherein both have the same LSR value. In a FC-based inverter system, the number of FCs used and their ratings determine the size and reliability of that system and hence serve as a major contributor to the overall cost of the system. Therefore, practical implementation of the proposed inverter is highly economical in view of significant reduction in the costs involved owing to only one in number FC being employed. This number is least among all other topologies wherein more FCs (between 2 and 3) are being used. In addition to reducing the number of FCs, there is a considerable decrease in voltage diversity factor as well, in comparison to other topologies. Further, the sensorless technique based FC voltage controller completely eliminates requirement for costly voltage feedback sensors, thereby obviating need for complex control algorithms like common mode control, model predictive control, and rule-based algorithms. Besides, all the power devices are not required to be operated at a higher frequency. This greatly enhances the overall efficiency of the proposed inverter. From the reliability point of view, if the FC H-bridge fails, the defective cell can be bypassed, and the inverter can be operated at its full power with reduced number

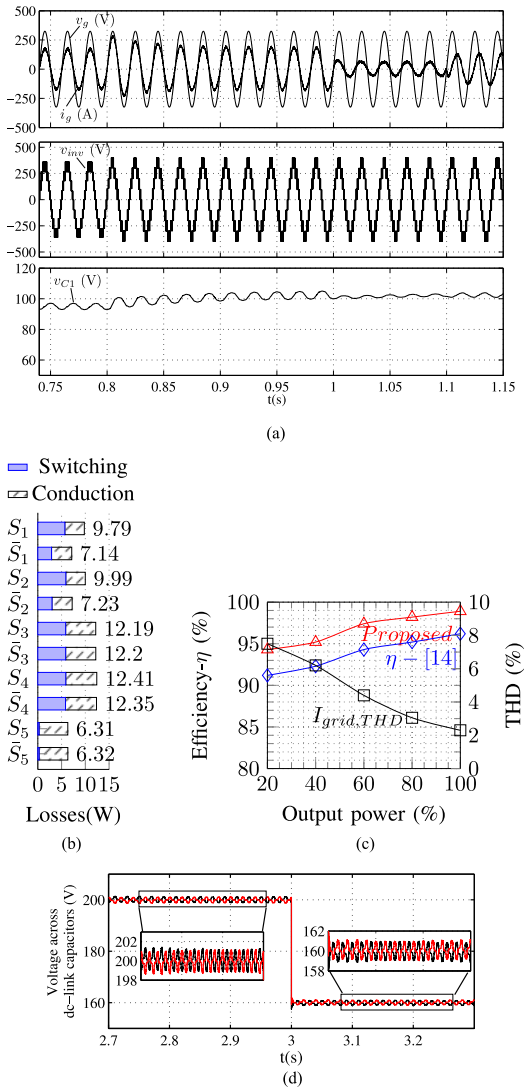

Fig. 3. Simulation results: (a) Grid voltage, grid current, FC voltage, output voltage for step change in dc-link voltage, and reference grid current. (b) Simulated switching, conduction, and total loss distribution. (c) Inverter efficiency and grid current THD for varying output power. (d) Voltage across dc-link capacitors for a step change in dc source amplitude.

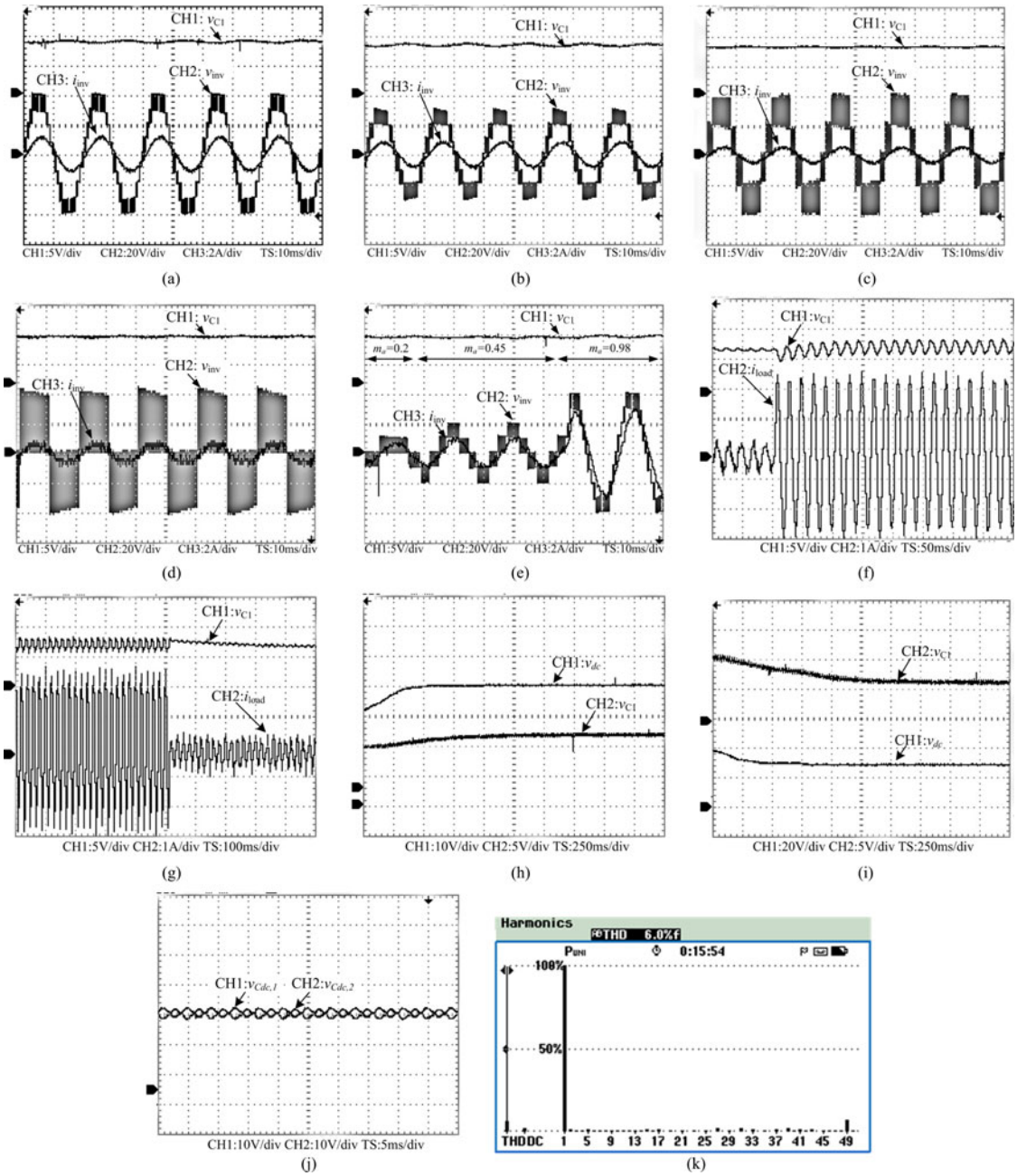

Fig. 4. Experimental results: (a) Voltage across FC, inverter output voltage, and load current for $m_a = 1$. (b) Voltage across FC, inverter output voltage, and load current for $m_a = 0.74$. (c) Voltage across FC, inverter output voltage, and load current for $m_a = 0.49$. (d) Voltage across FC, inverter output voltage, and load current for $m_a = 0.24$. (e) Voltage across FC, inverter output voltage, and current for step change in m_a. (f) Voltage across FC and load current with step increase of load. (g) Voltage across FC and load current with step decrease of load. (h) Voltage regulation during a fast 33% increase in dc source amplitude. (i) Voltage regulation during a fast 33% decrease in dc source amplitude. (j) Voltage across dc-link capacitors. (k) 9L inverter output voltage FFT analysis.

of levels. On the whole, the proposed hybrid inverter is therefore superior to most of the other inverter topologies, qualifying it as a preferred alternative for grid-connected renewable energy applications.

III. Simulation and Experimental Results

A. Simulation Results

A single-phase grid connected setup shown in Fig. 1 is simulated using MATLAB/Simulink to verify the performance of the proposed inverter with its sensorless control. A proportional resonant controller is employed to regulate the grid current at its set value. The main parameters are: rated power $P_g = 3$ kW; dc source voltage $V_{\rm dc} = 400$ V; fundamental grid frequency $f_g = 50$ Hz; carrier frequency $f_{\rm sw} = 2.5$ kHz; grid voltage $V_g = 230$ V; FC capacitance $C_1 = 2.5$ mF; filter inductance $L_f = 1.5$ mH; dc-link capacitance $C_{\rm dc,1} = C_{\rm dc,2} = 2.2$ mF. A balance booster/filter with series RLC configuration is employed for expediting the FC voltage balancing process. At $t = 0.8$ s, a step change of 360–400 V in $V_{\rm dc}$ is applied. The results

in Fig. 3(a) clearly illustrate the satisfactory performance of the proposed sensorless control in regulating the FC voltage to $V_{\rm dc}/4$ in spite of variation in dc-link voltage. Further, at $t = 1$ s, a step change in reference grid current is applied. It is apparent from the resulting waveform that the actual inverter current tracks the new reference value, as commanded within a cycle time, exhibiting high dynamic performance. At $t = 1.1$ s, the inverter is controlled to inject grid current at nonunity power factor, while exchanging reactive power with the grid, thereby proving its stable operation. Meanwhile, the FC voltage is observed to be well within its set value at all times. Further, analytical estimation of the switching losses, conduction losses, and total losses for the proposed inverter is carried out. The method described for power loss calculation in [29], which is based on extrapolation of the manufacturer's datasheet is employed. The power device used for the study is SKM100GB12T4 (SEMIKRON) with a rating of 1200 V, and 100 A. The simulated current through each device and their blocking voltage data are considered for the loss calculation. Fig. 3(c) depicts the loss distribution in the proposed inverter. The critical operating points of the converter are the maximum and minimum modulation indices at power factor PF $= 1$ and PF $= -1$, respectively. The loss distribution exhibits the biggest lack of balance at these points [30]. Moreover, the operating point at PF $= 1$ at rated power is considered since the typical operating PF of the grid-connected renewables is unity. As mentioned earlier, it can be observed that the LFS unit has negligible switching losses. This distinct loss distribution pattern aids in optimizing the proposed inverter by decreasing the semiconductor area of the lightly loaded device, resulting in further cost reduction. Fig. 3(d) shows the efficiency curve and the grid current THD over the percentage rated output power. From the plots, it can be inferred that the proposed inverter exhibits an improved efficiency over the RPC topology proposed in [14] and the injected grid current is in compliance with the harmonic limit specified by IEEE 519 Standard. The calculated inverter losses at unity power factor result in an inverter efficiency of 98.9%. Fig. 3(e) depicts the voltage across dc-link capacitors for a step change in dc source amplitude from 400 to 320 V. The symmetrical switching of the inverter results in the natural balancing of dc-link capacitors without the need for additional circuitry.

B. Experimental Results

A down-scaled prototype of the proposed inverter is built to validate its performance. Discrete IRFP250N MOSFETS are used as switching devices gated with TLP250 drivers. dSPACE DS1104 DSP is used as a core controller to implement the proposed control algorithm in real-time. A capacitance value of 1.1 mF is used for all the capacitors in the experiment. The dc-link voltage $V_{\rm dc}$ is set to 50 V and a resistive-inductive load ($R - L$) of 25 Ω and 5 mH is connected at the output. To appraise the performance of the proposed topology and its control, experimental results are elucidated. Fig. 4(a)–(d) shows the steady state voltage across FC, inverter output voltage, and load current for different modulation indices. It is evident from Fig. 4(e) that the FC voltage remains stabilized at its requisite value (12.5 V) against variations in the modulation indices. Further, the dynamic performance of the proposed inverter control with step increase and decrease in the load is shown in Fig. 4(f) and (g), respectively. The capacitor voltage ripple is found to be less than 8%. Fig. 4(h) shows that no precharged capacitor is required during startup. Also, the voltage across FC settles to its new value (10 V) smoothly, hence confirming its satisfactory performance. Fig. 4(i) illustrates the response of FC voltage for a rapid 33% decrease in dc source amplitude from 40 to 30 V. The voltage across the dc-link capacitors depicting the natural balancing property of the proposed inverter is shown in Fig. 4(j). The 9L output voltage THD is about 6% without any additional filters, as depicted in Fig. 4(k). The above mentioned simulations and experimental results confirm the applicability of the proposed inverter for all possible real-time operating conditions.

IV. Conclusion

Multilevel inverters are being developed and extensively exploited for generating high quality output voltages for numerous medium-voltage application fields. Applications urging a higher number of voltage levels escalate the number of components required. But use of high number of part counts in conventional multilevel inverters increases both the circuit intricacies as well as the control scheme involved, thereby resulting in higher cost implications and reduced reliability. Therefore, to subdue these disadvantages, this letter proposes a novel hybrid 9L inverter topology formed by cascading a TNPC and FC with two LFS connected across the dc-link. This is achieved using only ten power switches (among which two are operated at line frequency). Only one FC is incorporated in the circuit for generating the 9L output voltage. Further, it is confirmed that the proposed inverter structure has improved reliability and by cascading additional FCs, it can be effortlessly extended to obtain even higher number of voltage levels. In addition, a sensorless PWM technique based on the principle of energy balance for regulating the voltage of FC is suggested. An exhaustive review of recently proposed multilevel inverter topologies with RPC applicable for grid integration of renewable sources is carried out and the ensuing comparison certifies the merits of the proposed topology over conventional inverters. Comprehensive simulation results followed by hardware experimental results corresponding to steady state as well as transient conditions are presented to validate the practicability and potential prospects for extensive utilization of the proposed inverter with its sensorless voltage control for several grid-integrated applications using renewable energy systems.

References

[1] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[2] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[3] M. Calais, V. G. Agelidis, and M. Meinhardt, "Multilevel converters for single-phase grid connected photovoltaic systems: an overview," *Solar Energy*, vol. 66, no. 5, pp. 325–335, 1999.

[4] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.
[5] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.
[6] V. Agelidis, D. Baker, W. Lawrance, and C. Nayar, "A multilevel pwm inverter topology for photovoltaic applications," in *Proc. IEEE Int. Symp. Ind. Electron.*, 1997, vol. 2, pp. 589–594.
[7] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.
[8] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
[9] L. G. Franquelo *et al.*, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag*, vol. 2, no. 2, pp. 28–39, Jun. 2008.
[10] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, 2010.
[11] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: a review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, Aug. 2016.
[12] Y.-H. Liao and C.-M. Lai, "Newly-constructed simplified single-phase multistring multilevel inverter topology for distributed energy resources," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2386–2392, Sep. 2011.
[13] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2435–2443, Jun. 2011.
[14] J. Li, S. Bhattacharya, and A. Q. Huang, "A new nine-level active npc (ANPC) converter for grid connection of large wind turbines for distributed generation," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 961–972, Mar. 2011.
[15] G. Buticchi, D. Barater, E. Lorenzani, C. Concari, and G. Franceschini, "A nine-level grid-connected converter topology for single-phase transformerless pv systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3951–3960, Aug. 2014.
[16] V. Dargahi, A. K. Sadigh, G. K. Venayagamoorthy, and K. Corzine, "Hybrid double flying capacitor multicell converter and its application in grid-tied renewable energy resources," *IET Gener. Transmiss. Distrib.*, vol. 9, no. 10, pp. 947–956, 2015.
[17] T. Chaudhuri, P. Barbosa, P. Steimer, and A. Rufer, "Cross-connected intermediate level (CCIL) voltage source inverter," in *Proc. 2007 IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 490–496.
[18] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: A competitive solution for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 3, pp. 834–841, May/Jun. 2000.
[19] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 655–664, Mar. 2005.
[20] P. Rajeevan, K. Sivakumar, K. Gopakumar, C. Patel, and H. Abu-Rub, "A nine-level inverter topology for medium-voltage induction motor drive with open-end stator winding," *IEEE Trans. Power Electron.*, vol. 60, no. 9, pp. 3627–3636, Sep. 2013.
[21] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A nonconventional power converter for plasma stabilization," *IEEE Trans. Power Electron.*, vol. 5, no. 2, pp. 212–219, Apr. 1990.
[22] E. Najafi and A. H. M. Yatim, "Design and implementation of a new multilevel inverter topology," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4148–4154, Nov. 2012.
[23] H. Vahedi, P.-A. Labbé, and K. Al-Haddad, "Sensor-less five-level packed u-cell (PUC5) inverter operating in stand-alone and grid-connected modes," *IEEE Trans. Ind. Informat.*, vol. 12, no. 1, pp. 361–370, Feb. 2016.
[24] A. M. Ghias, J. Pou, G. J. Capella, V. G. Agelidis, R. P. Aguilera, and T. Meynard, "Single-carrier phase-disposition PWM implementation for multilevel flying capacitor converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5376–5380, Oct. 2015.
[25] N. Sandeep, P. Salodkar, and P. S. Kulkarni, "A new simplified multilevel inverter topology for grid-connected application," in *Proc. 2014 IEEE Elect., Electron. Comput. Sci.*, 2014, pp. 1–5.
[26] T. Chaudhuri, A. Rufer, and P. K. Steimer, "The common cross-connected stage for the 5l anpc medium voltage multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2279–2286, Jul. 2010.
[27] P. Barbosa, P. Steimer, L. Meysenc, M. Winkelnkemper, J. Steinke, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. 2005 IEEE 36th Power Electron. Spec. Conf.*, Jun. 2005, pp. 2296–2301.
[28] R. N. Viju, S. A. Rahul, R. S. Kaarthik, A. Kshirsagar, and K. Gopakumar, "Generation of higher number of voltage levels by stacking inverters of lower multilevel structures with low voltage devices for drives," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 52–59, Jan. 2017.
[29] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibanez, and J. L. Villate, "A comprehensive study of a hybrid modulation technique for the neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 294–304, Feb. 2009.
[30] D. Floricau, G. Gateau, M. Dumitrescu, and R. Teodorescu, "A new stacked NPC converter: 3L-topology and control," in *Proc. Power Electron. Appl., 2007 Eur. Conf.*, 2007, pp. 1–10.